Abstract of the Disclosure

A device to create, receive, and transmit packets of data in a packet switching network. This device employs a direct memory access packet controller which would interface between memory contained within a computer system and a packet switched network. This direct memory access packet controller would utilize one or more micro-engines that would dynamically allocate buffer space to process received packets of data. This direct memory access packet controller would further utilize a transmit cell FIFO circuit to allocate buffer space to packets being transmitted. In addition, a sequencer would act to control the workflow of packets being received and transmitted.